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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,459	10/17/2001	Ralf Schmitt	SUN-P5405	7393

7590 04/08/2003

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EXAMINER	
THOMPSON, ANNETTE M	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,459	SCHMITT ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-26* is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *27-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4)☐ Interview Summary (PTO-413) Paper No(s) _____
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other:

DETAILED ACTION

Applicants' Amendment and Response to Final Office Action has been examined. Claims 1, 7, 10, 15, 20, 21, and 26 are amended. Claims 27-36 are added. Claims 1-36 are pending.

Continued Examination Under 37 CFR 1.114

1. A Request for Continued Examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8 January 2003 has been entered.

Claim Rejections - 35 USC § 103

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of Claims 1-20

4. **Claims 1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Camporese et al. ("Camporese"), U.S. Patent 6,205,571 and Graef, U.S. Patent 6,305,001. Camporese discloses a clock tree distribution network for distributing a clock signal across a chip involving clock skew analysis. Although Camporese suggests Applicants' limitations, Camporese does not disclose a specific system for implementing the method. Graef also discloses a clock tree distribution planning method and additionally discloses a system for implementing the method that is a typical system used in IC designs. Graef further states that the system disclosed represents "one of many suitable computer platforms for implementing the method." (col. 15, ll. 47-50). Both Camporese and Graef disclose a method involving a clock distribution network.. However, Graef details the system that would be necessary to implement methods involving clock distribution networks in general. It therefore would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to use the system of Graef, or some similar system configuration, to implement the Camporese method.

5. Claims 15-18, 20, and 22-24 invoke the provisions of 35 U.S.C. 112, sixth paragraph and were considered accordingly.

6. Pursuant to claim 1 which recites a Clock Data Model (Fig. 2 illustrates this limitation; also, col. 3, ll. 48-50 discloses a clock-related electrical simulation model) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution comprising,

partitioning the complete clock net into a global clock net (the first level wiring networks, e.g. Figure 2, #201; reference the Fig. 2 description at col. 4, ll. 25-28) and a plurality of local clock nets (the second level of tree wires, e.g. Figure 2, #203; reference the Figure 2 description at col. 4, ll. 28-31);

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net: col. 12, ll. 12-23 wherein the twig wiring represents the local clock nets; additionally, the N_{sector} electrical lists comprise the loading for the plurality of local clock nets; simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets: col. 12, ll. 12-23 wherein the twig wiring represents the local clock nets; combining the plurality of simulations to form the complete clock net: col. 11, ll. 33-50; storing the plurality of simulations in the Clock Data Model: col. 11, ll. 19-22, wherein the tuned netlist represents the CDM with stored simulations, wherein the storing includes storing the simulated load for each point where the local clock net is connected to the global clock net (col. 11, ll. 10-14; col. 11, 19-26).

7. Pursuant to claim 2 wherein partitioning comprises breaking the complete clock net into equal sized parts according to rectangular grid coordinates: Figure 2 illustrates this limitation.

8. Pursuant to claim 3 wherein the method further comprises breaking at least one of the plurality of local clock nets down into at least one sub-local clock net: col. 4, ll. 28-31 suggests the existence of sub-local clock nets depending on the embodiment.

9. Pursuant to claim 4 wherein the method further comprises simulating the at least one sub-local clock net prior to simulating the corresponding local clock net: Fig. 7, step 735; col. 9, ll. 60-64.

10. Pursuant to claim 5 wherein at least two of the plurality of local clock nets are simulated in parallel: Creation of isolated net lists which represent local clock nets and are treated in parallel for tuning or simulation purposes, col. 9, ll. 8-27; see also col. 9, ll. 61-67 which discloses parallel tuning or simulation.

11. Pursuant to claim 6, wherein simulating the clock nets comprises extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database: the creation of the electrical netlist suggests this limitation, col. 6, ll. 10-65;

extracting component values of the elements of the local clock net from the microprocessor network database: col. 6, ll. 48-65;

simulating the local clock net based on the layout and the component values: col. 6, ll. 48-65;

extracting a load of the local clock net on the global clock net: col. 6, ll. 48-65.

12. Pursuant to claim 7 wherein simulating the local clock net comprises assuming that the clock arrival times form the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net: col. 9, ll. 35-43.

13. Pursuant to claim 8 wherein simulating the global clock net comprises extracting the layout of the global clock net from a microprocessor network database: the creation of the electrical netlist, col. 6, ll. 10-65, details the layout connections;

extracting component values of the elements of the global clock from the microprocessor network database: col. 6, ll. 48-65;

inserting the simulated loads of the plurality of local clock nets: col. 6, ll. 48-54; see also col. 7, ll. 13-15;

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads: col. 6, ll. 48-65.

14. Pursuant to claim 9 which further comprises evaluating the complete clock net to determine whether the results converge: col. 9, ll. 35-60, wherein the true point load response matrix is checked against the smoothed point load response matrix which has calculations of clock signal arrival times.

15. Pursuant to claim 10 wherein if the results do not converge, setting the clock arrival times to those calculated for the simulated global clock net: col. 9, lines 47-56;

re-simulating one of the plurality of local clock nets to generate a load for the local and global clock net: col. 12, ll. 12-23;

re-simulating the global clock net based at least on the simulated or re-simulated load of each of the plurality of local clock nets: col. 12, ll. 12-13 wherein the twig wiring represents the local clock nets.

combining the simulations and re-simulations to form the complete net: col. 11, ll. 33-50.

16. Pursuant to claim 11, wherein re-simulating the local clock net comprises re-simulating the local clock net based on the layout, the component values, and the calculated clock arrival times: col. 6, ll. 48-65;

extracting a load of the at least one local clock net on the global clock net: col. 6, ll. 48-65.

17. Pursuant to claim 12 wherein the method comprises re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net:

18. Pursuant to claim 13, wherein re-simulating the global clock net comprises inserting the simulated or re-simulated loads of the plurality of local clock nets (col. 6, ll. 48-54; see also col. 7, ll. 13-15;) and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads: col. 6, ll. 48-65.

19. Pursuant to claim 14, wherein the method further comprises storing the plurality of re-simulations in the Clock Data Model: col. 11, ll. 19-22.

20. Pursuant to Claim 15 which recites [a] Clock Data Model for use with a system for determining clock insertion delays for a microprocessor design having grid-based distribution, the system comprising means for partitioning the complete clock net into a global clock net and a plurality of local clock nets, means for simulating each of the plurality of local clock nets on the global clock net, means for simulating the global clock net based on the simulated load of each of the plurality of local clock nets and means for combining the plurality of simulations to form the complete clock net, the CDM comprising means for storing the simulation results (Graef discloses a system having all the ("means for")elements of this limitation at col. 15, line 42 to col. 17, line 4); wherein the means for storing the simulated load for each point is where the local clock net is connected to the global clock net (Camporese, col. 11, ll. 10-14; col. 11, 19-26)

21. Pursuant to claim 16 further comprising means for collecting all of the information created during the plurality of simulations: Graef, col. 16, ll. 19-37.

22. Pursuant to claim 17 further comprising means for retrieving all of the information created during the plurality of simulations: Graef, col. 16, ll. 48-53.

23. Pursuant to claim 18 further comprising means for querying all of the information created during the plurality of simulations: col. 16, ll. 38-47.

24. Pursuant to claim 19 further comprising a timing tool interface to provide accurate clock arrival times for each clocked element in the microprocessor design: col. 16, ll. 1-5.

25. Pursuant to claim 20 wherein the system further comprises means for evaluating the complete clock net to determine whether the results converge (col. 9, ll. 35-60), means for *determining* that clock arrival times are those calculated for the simulated global clock net, means for re-simulating at least one of the plurality of local clock nets to generate a load for at least one local clock net on the global clock net, means for simulating the global clock net based on the simulated or re-simulated load of each of the plurality of local clock nets, and means for combining the simulations and re-simulations to form the complete clock net and wherein the CDM further comprises means for storing the plurality of re-simulation results (Graef discloses a system having all the ("means for") elements of this limitation at col. 15, line 42 to col. 17, line 4).

Allowable Subject Matter

26. Claims 21-26 are allowed.

27. Claims 27-36 contain allowable subject matter.

28. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose a system for determining clock insertion delays for a microprocessor design with grid-based clock distribution that includes a local clock net simulator and global clock net simulator, a merging unit and a convergence evaluator unit. Further the prior art does not disclose a CDM as claimed wherein the clock arrival time and slope are stored for each point where the local clock net is connected to the global clock net.

Remarks

29. In this continued examination, Camporese at least suggests the added claim limitations. Therefore, the rejection of claims 1-20 under 35 U.S.C. 103(a) is sustained, herein, supra.

Conclusion

30. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703)306-3329.

31. Responses to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9318, (for **OFFICIAL** communications intended for entry)
(703)872-9319, (for Official **AFTER-FINAL** communications)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
Patent Examiner

7 April 2003